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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,593	03/17/2004	Chan-Yong Park	GAIN3.001AUS	3871

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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,593	PARK, CHAN-YONG	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *11-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-10* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 02/10/2005 has been entered.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 1-10, in the Paper filed 02/10/2005 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 03/17/2004 is acceptable.

Drawings

4. The formal drawings filed on 03/17/2004 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Applicant should please note that the listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the examiner has cited the references on form PTO-892, they have not been considered.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

8. Claim 8 recites the limitation "the InAlAs semiconductor layer" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 8 will be examined under the assumption (consistent with the specification) that "the InAlAs semiconductor layer" is a typo for – an InAlAs semiconductor layer –.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by TANAKA ET AL. (2002/0117697).

As a preliminary, it should be noted that Tanaka et al. disclose seven completely different devices: a first embodiment, shown at figure 1 and paragraphs 46-59, a second embodiment, shown at figure 7 and paragraphs 60-75, a "prior art" (to Tanaka et al.) embodiment, shown at figure 10 and paragraphs 5-7, a third embodiment, shown at figure 11 and paragraphs 76-89, a fourth embodiment, shown at figures 3 and 14 and paragraphs 90-98, a fifth embodiment, shown at figure 16 and paragraphs 99-103, and a sixth embodiment, shown at figure 19 and paragraphs 106-109. Only embodiments 2 (figure 7 and paragraphs 60-75) and 5 (figure 16 and paragraphs 99-103) are relevant to the current claim set.

A. With regard to claims 1-4, 8, and 10 the second embodiment of Tanaka et al. discloses a photodiode comprising a substrate 21 formed of one of a first conduction (n) type InP semiconductor layer and a semi-insulating InP semiconductor layer; a first conduction (n) type buffer layer 22 formed on a first surface of the substrate 21; an anti-reflection layer formed on a second surface of the substrate 21 which faces away from the first conduction (n) type buffer layer 22; a first electrode 31 formed to electrically contact the first conduction (n) type buffer layer 22 (note that the first electrode 31 is in electrical contact with first buffer 22 through

substrate 21); an amplifying layer 23, comprising at least one of an InAlAs semiconductor layer and an InAlGaAs semiconductor layer, formed on the first conduction (n) type buffer layer 22; a second conduction (p) type field controlling layer 24-26 formed on the amplifying layer 23; a second conduction (p) type ion injection (the term "ion injection" apparently referring to the ability of ion injection layer 25 to supply charge carriers to the photodiode while it operates) layer 25 formed within (between parts 24 and 26) the field controlling layer 24-26; a second conduction (p) type light-absorbing layer 27 formed on the field controlling layer 24-26; a second conduction (p) type buffer layer 28 formed on the light-absorbing layer 27; a second electrode 32 formed to electrically contact (note that the second electrode 32, like the first electrode 31, electrically contacts its respective buffer without physically contacting it. In this case Applicant's claim explicitly requires this arrangement – note the claimed location of the "ohmic contact layer") the second conduction (p) type buffer layer 28 through a second conduction (p) type ohmic contact layer 29 formed between the second conduction (p) type buffer layer 28 and the second electrode 32; and a passivation layer 33 covering a surface of the second conduction (p) type ohmic contact layer 29 and a surface of the first conduction (n) type buffer layer 22, while allowing the first electrode 31 to electrically contact the first conduction (n) type buffer layer 22 and the second electrode 32 to electrically contact the second conduction (p) type ohmic contact layer 29. Note figure 7 and paragraphs 62-66 of Tanaka et al.

B. With regard to claims 1-5 and 10 the fifth embodiment of Tanaka et al. discloses a photodiode with a substrate 251 formed of one of a first conduction (p) type InP semiconductor layer and a semi-insulating InP semiconductor layer; an InP first conduction (p) type buffer layer 252 formed on a first surface of the substrate 251; an anti-reflection layer 262 formed on a second surface of the substrate 251 which faces away from the first conduction (p) type buffer layer 252; a first electrode 260 formed to electrically contact the first conduction (p) type buffer layer 252; an amplifying layer 253 formed on the first conduction (p) type buffer layer 252; an InP second conduction (n) type field controlling layer 254-256 formed on the amplifying layer 253; a second conduction (n) type ion injection layer 255 formed within the field controlling layer 254-256; an InGaAs second conduction (n) type light-absorbing layer 257 formed on the field controlling layer 254-256; an InP second conduction (n) type buffer layer 258 formed on the light-absorbing layer 257; a second electrode 261 formed to electrically contact the second conduction (n) type buffer layer 258 through a second conduction (n) type ohmic contact layer 259 formed between the second conduction (n) type buffer layer 258 and the second electrode 261; and a passivation layer 209 covering a surface of the second conduction (n) type ohmic contact layer 259 and a surface of the first conduction (p) type buffer layer 252, while allowing the first electrode 260 to electrically contact the first conduction (p) type buffer layer 252 and the second electrode 261 to electrically contact the second conduction (n)

type ohmic contact layer 259. Note figure 16 and paragraphs 101-102 of Tanaka et al.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over TANAKA ET AL. (2002/0117697) in view of CLARK (4,326,211).

Tanaka et al. discloses two different photodiodes, each with all the limitations of claims 6 and 9 except a first conduction type buffer layer comprising both an InP semiconductor layer and an InAlAs semiconductor layer and a second electrode formed in a ring structure so as to project a plurality of optical signals toward the second electrode. Note figures 7,16 and paragraphs 62 and 101 of Tanaka et al.

Clark discloses a photodiode having a first conduction type (n-type) buffer layer comprising n type InP semiconductor layer 101 and n+ InAlAs semiconductor layer 102 that is located adjacent to the multiplication region of the photodiode to provide a depletion stop at the n-side of the active portion of the photodiode. Clark also discloses a metal ring electrode 111 for exposing a light-absorbing re-

gion to incoming light, which allows the electrode to project a plurality of optical signals. Note figures 2 and 3; column 4 lines 15,16, and 26-33; and column 6 line 1 of Clark. Therefore, it would have been obvious to a person having skill in the art to augment of Tanaka et al.'s photodiode with the first conduction type buffer layer comprising an InP semiconductor layer and an InAlAs semiconductor layer and the second (p-side) electrode formed in a ring structure so as to project a plurality of optical signals toward the second electrode, such as taught by Clark in order, in the case of the first conduction type buffer layer, to provide a depletion stop at the n-side of the active portion of the photodiode, and, in the case of the ring-structured electrode, to expose the light absorbing region to incoming light, to thus provide a way to prevent electric field punch-through and resultant non-optically generated current, and to allow the light absorbing region access to light..

Allowable Subject Matter

11. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

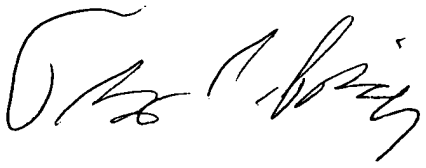
Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is

571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
03/05